WE CLAIM:

1. An integrated circuit comprising:
a data processing circuit operable to perform data processing operations;
a processor operable to perform data processing operations under program instruction control; and
a diagnostic circuit coupled to said data processing circuit and operable to capture diagnostic data relating to said data processing circuit; wherein
said processor is also coupled to said diagnostic circuit and is operable to access said diagnostic data relating to said data processing circuit independently of said data processing circuit.

2. An integrated circuit as claimed in claim 1, wherein said diagnostic circuit is operable upon detecting predetermined conditions to halt data processing by said data processing circuit to provide halting mode debug.

3. An integrated circuit as claimed in claim 1, wherein said diagnostic circuit is operable to capture diagnostic code profiling data relating to program instructions being executed by said data processing circuit whilst said data processing circuit continues to execute program instructions.

4. An integrated circuit as claimed in claim 1, wherein said diganostic circuit is operable upon detecting predetermined conditions to trigger said data processing circuit to execute an exception handling program to provide monitor mode debug.

5. An integrated circuit as claimed in claim 1, wherein said processor is operable to control output of said diagnostic data relating to said data processing circuit from said integrated circuit.

6. An integrated circuit as claimed in claim 1, wherein said processor is operable to control said diagnostic circuit to perform diagnostic operations upon said data processing circuit.

7. An integrated circuit as claimed in claim 1, wherein said data processing circuit and said processor communicate during non-diagnostic operation via a system bus.

8. An integrated circuit as claimed in claim 1, wherein said data processing circuit and said processor communicate during diagnostic operation via a diagnostic bus.

9. An integrated circuit as claimed in claim 7, comprising a bus bridge between said system bus and a diagnostic bus, said data processing circuit and said processor communicating during diagnostic operation via said system bus, said bus bridge and said diagnostic bus.

10. An integrated circuit as claimed in claim 1, wherein said diagnostic circuit is operable to store said diagnostic data relating to said data processing circuit within memory mapped storage locations accessible by said processor.

11. An integrated circuit as claimed in claim 1, comprising:
a processor diagnostic circuit coupled to said processor and operable upon detecting predetermined conditions to halt program instruction execution by said processor and capture diagnostic data relating to said processor; wherein
said data processing circuit is also coupled to said processor diagnostic circuit and is operable to access said diagnostic data said relating to said processor.

12. An integrated circuit as claimed in claim 1, comprising a peripheral device communication circuit operable during non-diagnostic operation of said integrated circuit to provide data communication with an external operational device coupled to said integrated circuit, said peripheral device communication circuit being used by said processor during diagnostic operation to communicate at least one of said diagnostic data relating to said data processing circuit, diagnostic operations and pre-processed diagnostic data with an external diagnostic device.

13. An integrated circuit as claimed in claim 9, wherein said bus bridge is coupled via a diagnostic interface to an external diagnostic device.

14. An integrated circuit as claimed in claim 1, wherein said data processing circuit is a further processor operable to perform data processing operations under program instruction control.

15. A method of obtaining diagnostic data for an integrated circuit comprising the steps of:

performing data processing operations with a data processing circuit within said integrated circuit;

performing data processing operations under program instruction control with a processor within said integrated circuit;

capturing with a diagnostic circuit coupled to said data processing circuit and within said integrated circuit diagnostic data relating to said data processing circuit; and

accessing said diagnostic data said relating to said data processing circuit with said processor and independently of said data processing circuit.

16. A method as claimed in claim 15, wherein said diagnostic circuit is operable upon detecting predetermined conditions to halt data processing by said dat aprocessing circuit to provide halting mode debug.

17. A method as claimed in claim 15, wherein said diagnostic circuit is operable to capture diagnostic code profiling data relating to program instructions being executed by said data processing circuit whilst said data processing circuit continues to execute program instructions.

18. A method as claimed in claim 15, wherein said diagnostic circuit is operable upon detecting predetermined conditions to trigger said data processing circuit to execute an exception handling program to provide monitor mode debug.

19. A method as claimed in claim 15, wherein said processor is operable to control output of said diagnostic data relating to said data processing circuit from said integrated circuit.

20. A method as claimed in claim 15, wherein said processor is operable to control said diagnostic circuit to perform diagnostic operations upon said data processing circuit.

21. A method as claimed in claim 15, wherein said data processing circuit and said processor communicate during non-diagnostic operation via a system bus.

22. A method as claimed in claim 15, wherein said data processing circuit and said processor communicate during diagnostic operation via a diagnostic bus.

23. A method as claimed in claim 21, wherein said data processing circuit and said processor communicate during diagnostic operation via said system bus, a bus bridge and a diagnostic bus.

24. A method as claimed in claim 15, wherein said diagnostic circuit is operable to store said diagnostic data relating to said data processing circuit within memory mapped storage locations accessible by said processor.

25. A method as claimed in claim 15, wherein:
a processor diagnostic circuit is coupled to said processor is operable upon detecting predetermined conditions to halt program instruction execution by said processor and to capture diagnostic data relating to said processor; and
said data processing circuit is also coupled to said processor diagnostic circuit and is operable to access said diagnostic data said relating to said processor.

26. A method as claimed in claim 15, wherein a peripheral device communication circuit is operable during non-diagnostic operation of said integrated circuit to provide data communication with an external operational device coupled to said integrated circuit, said peripheral device communication circuit being used by said processor

during diagnostic operation to communicate at least one of said diagnostic data relating to said data processing circuit, diagnostic operations and pre-processed diagnostic data with an external diagnostic device.

27. A method as claimed in claim 23, wherein said bus bridge is coupled via a diagnostic interface to an external diagnostic device.

28. A method as claimed in claim 15, wherein said data processing circuit is a further processor operable to perform data processing operations under program instruction control.

29. A computer program product having a computer program operable to control a processor to obtain diagnostic data for an integrated circuit in accordance with the method of claim 15.